PRELIMINARY DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD70F3040, 70F3040Y

V850/SV1™
32-/16-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD70F3040 and μPD70F3040Y are products that substitute flash memory for the mask ROM of the μPD703039, 703040, 703041 and μPD703039Y, 703040Y, 703041Y, respectively. Since the μPD70F3040 and 70F3040Y can be read and written while mounted on the board, these products are ideal for evaluation during system development, multiple-version small-scale production or quick product release.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V850/SV1 User's Manual Hardware: U14462E
V850 Family™ User's Manual Architecture: U10243E

FEATURES

- Pin compatible with μPD703039, 703040, 703041, 703039Y, 703040Y, and 703041Y
  - For mass production, these can be replaced by a mask ROM version.
    μPD70F3040 → μPD703039, 703040, 703041
    μPD70F3040Y → μPD703039Y, 703040Y, 703041Y

ORDERING INFORMATION

Part Number	Package
μPD70F3040GM-UEU	176-pin plastic LQFP (fine-pitch) (24 × 24 mm)
μPD70F3040YGM-UEU	176-pin plastic LQFP (fine-pitch) (24 × 24 mm)

DIFFERENCES BETWEEN V850/SV1 PRODUCTS

	Internal ROM	Internal RAM	I^2C	V_{PP} Pin
μPD70F3040	256 KB (flash memory)	16 KB	None	Provided
μPD70F3040Y			Provided	
μPD703039	256 KB (mask ROM)	8 KB	None	None
μPD703039Y			Provided	
μPD703040		16 KB	None	
μPD703040Y			Provided	
μPD703041	192 KB (mask ROM)	8 KB	None	
μPD703041Y			Provided	

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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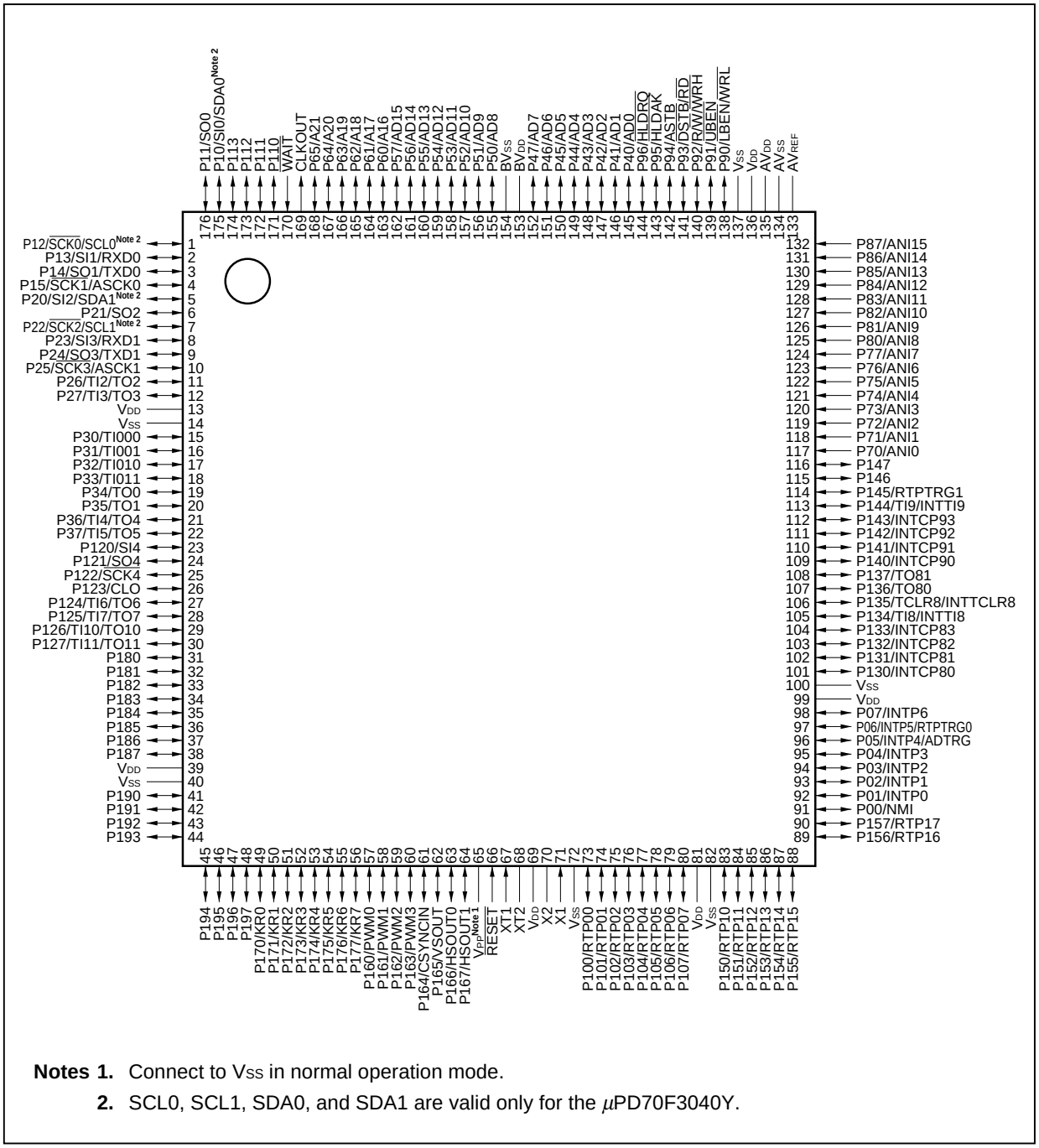
PIN CONFIGURATION

176-pin plastic LQFP (fine-pitch) (24 × 24 mm)

μPD70F3040GM-UEU

μPD70F3040YGM-UEU



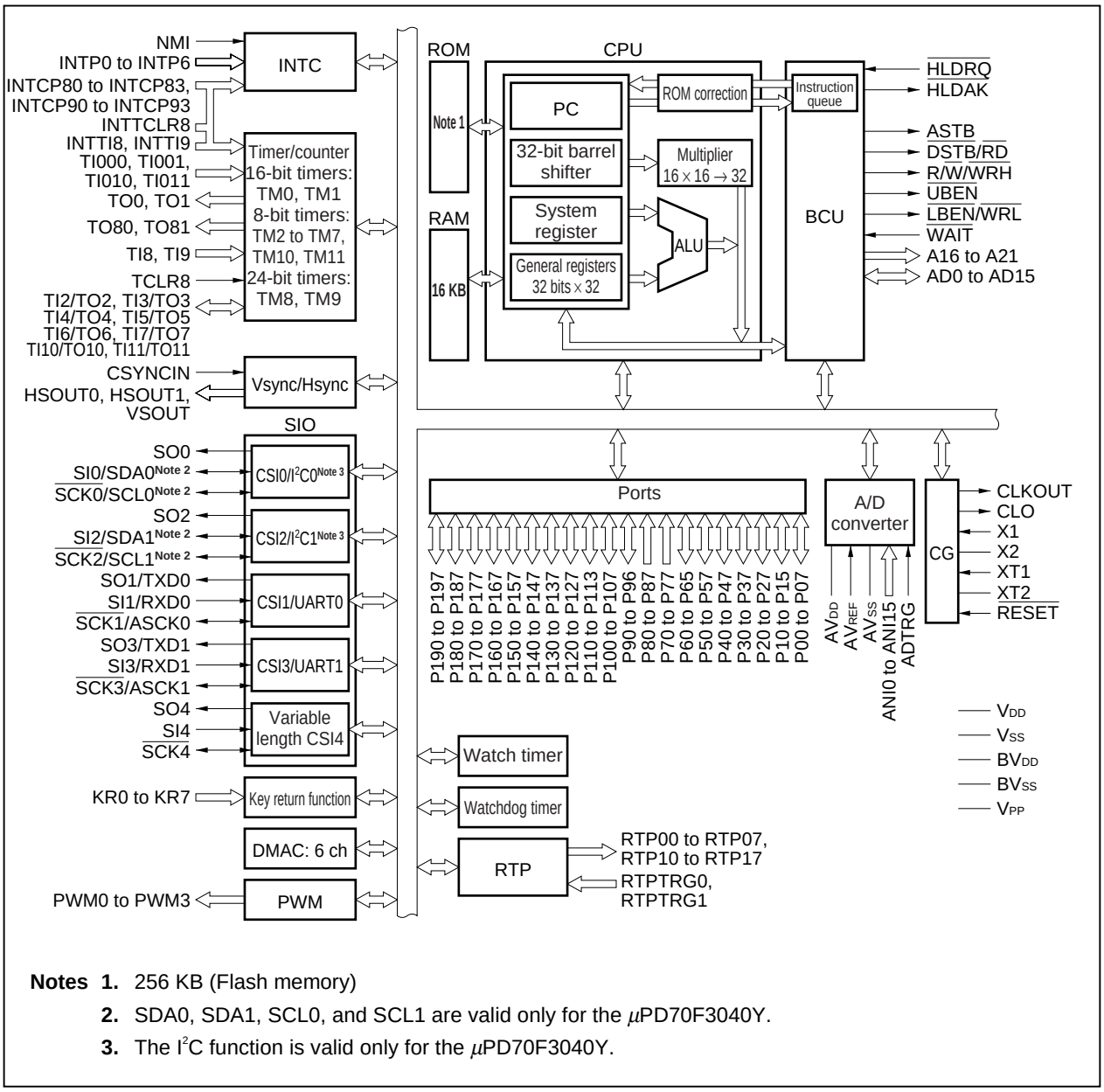
Notes 1. Connect to V_{SS} in normal operation mode.

2. SCL0, SCL1, SDA0, and SDA1 are valid only for the μPD70F3040Y.

PIN IDENTIFICATION

A16 to A21:	Address Bus
AD0 to AD15:	Address/Data Bus
ADTRG:	AD Trigger Input
ANI0 to ANI15:	Analog Input
ASCK0, ASCK1:	Asynchronous Serial Clock
ASTB:	Address Strobe
AV_{DD}:	Analog Power Supply
AV_{REF}:	Analog Reference Voltage
AV_{SS}:	Analog Ground
BV_{DD}:	Bus Interface Power Supply
BV_{SS}:	Bus Interface Ground
CLKOUT:	Clock Output
CLO:	Clock Output (divided)
CSYNCIN:	Csync Input
$\overline{DSTB}$:	Data Strobe
$\overline{HLDAK}$:	Hold Acknowledge
$\overline{HLDRQ}$:	Hold Request
HSOUT0, HSOUT1:	Hsync Output
INTCP80 to INTCP83,:	Interrupt Request from Peripherals
INTCP90 to INTCP93,	
INTP0 to INTP6,	
INTTCLR8,	
INTTI8, INTTI9	
KR0 to KR7:	Key Return
$\overline{LBEN}$:	Lower Byte Enable
NMI:	Non-Maskable Interrupt Request
P00 to P07:	Port 0
P10 to P15:	Port 1
P20 to P27:	Port 2
P30 to P37:	Port 3
P40 to P47:	Port 4
P50 to P57:	Port 5
P60 to P65:	Port 6
P70 to P77:	Port 7
P80 to P87:	Port 8
P90 to P96:	Port 9
P100 to P107:	Port 10
P110 to P113:	Port 11
P120 to P127:	Port 12
P130 to P137:	Port 13
P140 to P147:	Port 14
P150 to P157:	Port 15
P160 to P167:	Port 16
P170 to P177:	Port 17
P180 to P187:	Port 18
P190 to P197:	Port 19
PWM0 to PWM3:	Pulse Width Modulation
$\overline{RD}$:	Read
$\overline{RESET}$:	Reset
RTP00 to RTP07,:	Real-time Output Port
RTP10 to RTP17	
RTPTRG0, RTPTRG1:	RTP Trigger Input
R/$\overline{W}$:	Read/Write Status
RXD0, RXD1:	Receive Data
$\overline{SCK0}$ to $\overline{SCK4}$:	Serial Clock
SCL0, SCL1:	Serial Clock
SDA0, SDA1:	Serial Data
SI0 to SI4:	Serial Input
SO0 to SO4:	Serial Output
TCLR8:	Timer Clear
TI000, TI001, TI010,:	Timer Input
TI011, TI2 to TI11	
TO0 to TO7, TO80,:	Timer Output
TO81, TO10, TO11	
TXD0, TXD1:	Transmit Data
$\overline{UBEN}$:	Upper Byte Enable
V_{DD}:	Power Supply
V_{PP}:	Programming Power Supply
VSOUT:	Vsync Output
V_{SS}:	Ground
$\overline{WAIT}$:	Wait
$\overline{WRH}$:	Write Strobe High Level Data
$\overline{WRL}$:	Write Strobe Low Level Data
X1, X2:	Crystal for Main System Clock
XT1, XT2:	Crystal for Subsystem Clock

INTERNAL BLOCK DIAGRAM



Notes 1. 256 KB (Flash memory)

2. SDA0, SDA1, SCL0, and SCL1 are valid only for the μPD70F3040Y.

3. The I^2C function is valid only for the μPD70F3040Y.

CONTENTS

1. PIN FUNCTIONS

1.1 Port Pins

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Pin Name	I/O	PULL	Function	Alternate Function
P00	I/O	Yes	Port 0 8-bit I/O port Input/output mode can be specified in 1-bit units.	NMI
P01				INTP0
P02				INTP1
P03				INTP2
P04				INTP3
P05				INTP4/ADTRG
P06				INTP5/RTPTRG0
P07				INTP6
P10	I/O	Yes	Port 1 6-bit I/O port Input/output mode can be specified in 1-bit units.	SI0/SDA0
P11				SO0
P12				$\overline{\text{SCK0}}$/SCL0
P13				SI1/RXD0
P14				SO1/TXD0
P15				$\overline{\text{SCK1}}$/ASCK0
P20	I/O	Yes	Port 2 8-bit I/O port Input/output mode can be specified in 1-bit units.	SI2/SDA1
P21				SO2
P22				$\overline{\text{SCK2}}$/SCL1
P23				SI3/RXD1
P24				SO3/TXD1
P25				$\overline{\text{SCK3}}$/ASCK1
P26				TI2/TO2
P27				TI3/TO3
P30	I/O	Yes	Port 3 8-bit I/O port Input/output mode can be specified in 1-bit units.	TI000
P31				TI001
P32				TI010
P33				TI011
P34				TO0
P35				TO1
P36				TI4/TO4
P37				TI5/TO5
P40	I/O	No	Port 4 8-bit I/O port Input/output mode can be specified in 1-bit units.	AD0
P41				AD1
P42				AD2
P43				AD3
P44				AD4

Remark PULL: On-chip pull-up resistor

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Pin Name	I/O	PULL	Function	Alternate Function
P45	I/O	No	Port 4 8-bit I/O port Input/output mode can be specified in 1-bit units.	AD5
P46				AD6
P47				AD7
P50	I/O	No	Port 5 8-bit I/O port Input/output mode can be specified in 1-bit units.	AD8
P51				AD9
P52				AD10
P53				AD11
P54				AD12
P55				AD13
P56				AD14
P57				AD15
P60	I/O	No	Port 6 6-bit I/O port Input/output mode can be specified in 1-bit units.	A16
P61				A17
P62				A18
P63				A19
P64				A20
P65				A21
P70	Input	No	Port 7 8-bit input port	ANI0
P71				ANI1
P72				ANI2
P73				ANI3
P74				ANI4
P75				ANI5
P76				ANI6
P77				ANI7
P80	Input	No	Port 8 8-bit input port	ANI8
P81				ANI9
P82				ANI10
P83				ANI11
P84				ANI12
P85				ANI13
P86				ANI14
P87				ANI15
P90	I/O	No	Port 9 7-bit I/O port Input/output mode can be specified in 1-bit units.	$\overline{\text{LBEN}}$/$\overline{\text{WRL}}$
P91				$\overline{\text{UBEN}}$
P92				R/$\overline{\text{W}}$/$\overline{\text{WRH}}$
P93				$\overline{\text{DSTB}}$/$\overline{\text{RD}}$

Remark PULL: On-chip pull-up resistor

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Pin Name	I/O	PULL	Function	Alternate Function
P94	I/O	No	Port 9 7-bit I/O port Input/output mode can be specified in 1-bit units.	ASTB
P95				$\overline{\text{HLDAK}}$
P96				$\overline{\text{HLDRQ}}$
P100	I/O	Yes	Port 10 8-bit I/O port Input/output mode can be specified in 1-bit units.	RTP00
P101				RTP01
P102				RTP02
P103				RTP03
P104				RTP04
P105				RTP05
P106				RTP06
P107				RTP07
P110	I/O	No	Port 11 4-bit I/O port Input/output mode can be specified in 1-bit units.	–
P111				–
P112				–
P113				–
P120	I/O	No	Port 12 8-bit I/O port Input/output mode can be specified in 1-bit units.	SI4
P121				SO4
P122				$\overline{\text{SCK4}}$
P123				CLO
P124				TI6/TO6
P125				TI7/TO7
P126				TI10/TO10
P127				TI11/TO11
P130	I/O	No	Port 13 8-bit I/O port Input/output mode can be specified in 1-bit units.	INTCP80
P131				INTCP81
P132				INTCP82
P133				INTCP83
P134				TI8/INTTI8
P135				TCLR8/INTTCLR8
P136				TO80
P137				TO81
P140	I/O	No	Port 14 8-bit I/O port Input/output mode can be specified in 1-bit units.	INTCP90
P141				INTCP91
P142				INTCP92
P143				INTCP93
P144				TI9/INTTI9
P145				RTPTRG1
P146				–
P147				–

Remark PULL: On-chip pull-up resistor

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Pin Name	I/O	PULL	Function	Alternate Function
P150	I/O	No	Port 15 8-bit I/O port Input/output mode can be specified in 1-bit units.	RTP10
P151				RTP11
P152				RTP12
P153				RTP13
P154				RTP14
P155				RTP15
P156				RTP16
P157				RTP17
P160	I/O	No	Port 16 8-bit I/O port Input/output mode can be specified in 1-bit units.	PWM0
P161				PWM1
P162				PWM2
P163				PWM3
P164				CSYNCIN
P165				VSOUT
P166				HSOUT0
P167				HSOUT1
P170	I/O	Yes	Port 17 8-bit I/O port Input/output mode can be specified in 1-bit units.	KR0
P171				KR1
P172				KR2
P173				KR3
P174				KR4
P175				KR5
P176				KR6
P177				KR7
P180	I/O	No	Port 18 8-bit I/O port Input/output mode can be specified in 1-bit units.	–
P181				–
P182				–
P183				–
P184				–
P185				–
P186				–
P187				–
P190	I/O	No	Port 19 8-bit I/O port Input/output mode can be specified in 1-bit units.	–
P191				–
P192				–
P193				–
P194				–
P195				–
P196				–
P197				–

Remark PULL: On-chip pull-up resistor

1.2 Non-Port Pins

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Pin Name	I/O	PULL	Function	Alternate Function
A16 to A21	Output	No	Address bus 16 to 21	P60 to P65
AD0 to AD7	I/O	No	Address/data multiplexed bus 0 to 15	P40 to P47
AD8 to AD15				P50 to P57
ADTRG	Input	Yes	A/D converter external trigger input	P05/INTP4
ANI0 to ANI7	Input	No	Analog input to A/D converter	P70 to P77
ANI8 to ANI15	Input	No		P80 to P87
ASCK0	Input	Yes	Baud rate clock input for UART0 and UART1	P15/$\overline{\text{SCK1}}$
ASCK1				P25/$\overline{\text{SCK3}}$
ASTB	Output	No	External address strobe signal output	P94
AV_{DD}	–	–	Positive power supply for A/D converter and ports used for alternate functions	–
AV_{REF}	Input	–	Reference voltage input for A/D converter	–
AV_{SS}	–	–	Ground potential for A/D converter and ports used for alternate functions	–
BV_{DD}	–	–	Positive power supply for bus interface and ports used for alternate functions	–
BV_{SS}	–	–	Ground potential for bus interface and ports used for alternate functions	–
CLKOUT	Output	–	Internal system clock output	–
CLO	Output	No	CLO output signal	P123
CSYNCIN	Input	No	Csync signal input	P164
$\overline{\text{DSTB}}$	Output	No	External data strobe signal output	P93/$\overline{\text{RD}}$
$\overline{\text{HLDAK}}$	Output	No	Bus hold acknowledge output	P95
$\overline{\text{HLDRQ}}$	Input	No	Bus hold request input	P96
HSOUT0	Output	No	Hsync signal output before compensation	P166
HSOUT1			Hsync signal output after compensation	P167
INTCP80 to INTCP83	Input	No	External capture input for CC80 to CC83	P130 to P133
INTCP90 to INTCP93	Input	No	External capture input for CP90 to CP93	P140 to P143
INTP0 to INTP3	Input	Yes	External interrupt request input (analog noise elimination)	P01 to P04
INTP4			External interrupt request input (digital noise elimination)	P05/ADTRG
INTP5				P06/RTPTRG0
INTP6			External interrupt request input (digital noise elimination supporting remote controller)	P07

Remark PULL: On-chip pull-up resistor

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Pin Name	I/O	PULL	Function	Alternate Function
INTTCLR8	Input	No	External interrupt request input (digital noise elimination)	P135/TCLR8
INTTI8	Input	No		P134/TI8
INTTI9				P144/TI9
KR0 to KR7	Input	Yes	Key return input	P170 to P177
$\overline{\text{LBEN}}$	Output	No	Lower byte enable signal output for external data bus	P90/$\overline{\text{WRL}}$
NMI	Input	Yes	Non-maskable interrupt request input	P00
PWM0 to PWM3	Output	No	Output of PWM channels 0 to 3	P160 to P163
$\overline{\text{RD}}$	Output	No	Bus read strobe signal output	P93/$\overline{\text{DSTB}}$
$\overline{\text{RESET}}$	Input	–	System reset input	–
RTP00 to RTP07	Output	Yes	Real-time output port	P100 to P107
RTP10 to RTP17				P150 to P157
RTPTRG0	Input	Yes	RTP external trigger input	P06
RTPTRG1		No		P146
R/$\overline{\text{W}}$	Output	No	External read/write status output	P92/$\overline{\text{WRH}}$
RXD0	Input	Yes	Serial receive data input for UART0 and UART1	P13/SI1
RXD1				P23/SI3
$\overline{\text{SCK0}}$	I/O	Yes	Serial clock I/O for CSI0 to CSI3 (3-wire mode)	P12/SCL0
$\overline{\text{SCK1}}$				P15/ASCK0
$\overline{\text{SCK2}}$				P22/SCL1
$\overline{\text{SCK3}}$				P25/ASCK1
$\overline{\text{SCK4}}$		No	Variable-length CSI4 serial clock I/O	P122
SCL0	I/O	Yes	Serial clock I/O for I^2C0 and I^2C1 (μPD70F3040Y)	P12/$\overline{\text{SCK0}}$
SCL1				P22/$\overline{\text{SCK2}}$
SDA0	I/O	Yes	Serial transmit/receive data I/O for I^2C0 and I^2C1 (μPD70F3040Y)	P10/SI0
SDA1				P20/SI2
SI0	Input	Yes	Serial receive data input for CSI0 to CSI3 (3-wire mode)	P10/SDA0
SI1				P13/RXD0
SI2				P20/SDA1
SI3				P23/RXD1
SI4		No	Variable-length CSI4 serial receive data input (3-wire mode)	P120
SO0	Output	Yes	Serial transmit data output for CSI0 to CSI3	P11
SO1				P14/TXD0
SO2				P21
SO3				P24/TXD1
SO4		No	Variable-length CSI4 serial transmit data output	P121
TCLR8	Input	No	External clear input for TM8	P135/INTTCLR8

Remark PULL: On-chip pull-up resistor

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Pin Name	I/O	PULL	Function	Alternate Function
TI000	Input	Yes	External count clock input/external capture trigger input for TM0	P30
TI001			External capture trigger input for TM0	P31
TI010			External count clock input/external capture trigger input for TM1	P32
TI011			External capture trigger input for TM1	P33
TI2			External count clock input for TM2	P26/TO2
TI3			External count clock input for TM3	P27/TO3
TI4			External count clock input for TM4	P36/TO4/A15
TI5			External count clock input for TM5	P37/TO5
TI6		No	External count clock input for TM6	P124/TO6
TI7			External count clock input for TM7	P125/TO7
TI8			External count clock input for TM8	P134/INTTI8
TI9			External count clock input for TM9	P144/INTTI9
TI10			External count clock input for TM10	P126/TO10
TI11			External count clock input for TM11	P127/TO11
TO0	Output	Yes	Pulse signal output for TM0	P34
TO1			Pulse signal output for TM1	P35
TO2			Pulse signal output for TM2	P26/TI2
TO3			Pulse signal output for TM3	P27/TI3
TO4			Pulse signal output for TM4	P36/TI4
TO5			Pulse signal output for TM5	P37/TI5
TO6		No	Pulse signal output for TM6	P124/TI6
TO7			Pulse signal output for TM7	P125/TI7
TO80			Pulse signal output 0 for TM8	P136
TO81			Pulse signal output 1 for TM8	P137
TO10			Pulse signal output for TM10	P126/TI10
TO11			Pulse signal output for TM11	P127/TI11
TXD0	Output	Yes	Serial transmit data output for UART0 and UART1	P14/SO1
TXD1				P24/SO3
$\overline{\text{UBEN}}$	Output	No	Higher byte enable signal output for external data bus	P91
V_{DD}	–	–	Positive power supply pin	–
V_{PP}	–	–	High voltage application pin for program write/verify	–
VSOUT	Output	No	Vsync signal output	P165
V_{SS}	–	–	Ground potential	–
$\overline{\text{WAIT}}$	Input	No	External $\overline{\text{WAIT}}$ signal input	–
$\overline{\text{WRH}}$	Output	No	Higher byte write strobe signal output for external data bus	P92/R/$\overline{\text{W}}$
$\overline{\text{WRL}}$			Lower byte write strobe signal output for external data bus	P90/$\overline{\text{LBEN}}$

Remark PULL: On-chip pull-up resistor

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Pin Name	I/O	PULL	Function	Alternate Function
X1	Input	No	Resonator connection for main system clock	–
X2	–			–
XT1	Input	No	Resonator connection for subsystem clock	–
XT2	–			–

Remark PULL: On-chip pull-up resistor

1.3 Pin I/O Circuits, I/O Buffer Supply, and Recommended Connection of Unused Pins

Table 1-1 shows the input/output circuit type of each pin and the recommended connection of unused pins.
For the input/output configuration of each type, refer to Figure 1-1.

Table 1-1. Types of Pin I/O Circuit and Recommended Connection of Unused Pins (1/2)

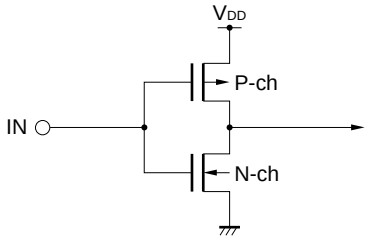
Pin	Alternate Function	I/O Circuit Type	I/O Buffer Power Supply	Recommended Connection Method
P00	NMI	5-W	V_{DD}	Input: Independently connect to V_{DD} or V_{SS} via a resistor Output: Leave open
P01 to P04	INTP0 to INTP3			
P05	INTP4/ADTRG			
P06	INTP5/RTPTRG0			
P07	INTP6			
P10	SI0/SDA0	10-F	V_{DD}	
P11	SO0	10-E		
P12	$\overline{SCK0}$/SCL0	10-F		
P13	SI1/RXD0	5-W		
P14	SO1/TXD0	10-E		
P15	$\overline{SCK1}$/ASCK0	10-F		
P20	SI2/SDA1	10-F	V_{DD}	
P21	SO2	10-E		
P22	$\overline{SCK2}$/SCL1	10-F		
P23	SI3/RXD1	5-W		
P24	SO3/TXD1	10-E		
P25	$\overline{SCK3}$/ASCK1	10-F		
P26, P27	TI2/TO2, TI3/TO3	5-W		
P30, P31	TI000, TI001	5-W	V_{DD}	
P32, P33	TI010, TI011			
P34, P35	TO0, TO1	5-A		
P36	TI4/TO4	5-W		
P37	TI5/TO5			
P40 to P47	AD0 to AD7	5	BV_{DD}	Input: Independently connect to BV_{DD} or BV_{SS} via a resistor Output: Leave open
P50 to P57	AD8 to AD15	5	BV_{DD}	
P60 to P65	A16 to A21	5	BV_{DD}	
P70 to P77	ANI0 to ANI7	9	AV_{DD}	Connect to AV_{SS}
P80 to P87	ANI8 to ANI15	9	AV_{DD}	
P90	$\overline{LBEN}$/$\overline{WRL}$	5	BV_{DD}	Input: Independently connect to BV_{DD} or BV_{SS} via a resistor Output: Leave open
P91	$\overline{UBEN}$			
P92	R/$\overline{W}$/$\overline{WRH}$			
P93	$\overline{DSTB}$/$\overline{RD}$			
P94	ASTB			
P95	$\overline{HLDAK}$			
P96	$\overline{HLDRQ}$			
P100 to P107	RTP00 to RTP07	10-E	V_{DD}	Input: Independently connect to V_{DD} or V_{SS} via a resistor Output: Leave open
P110 to P113	–	5	V_{DD}	
P120	SI4	5-K	V_{DD}	

Table 1-1. Types of Pin I/O Circuit and Recommended Connection of Unused Pins (2/2)

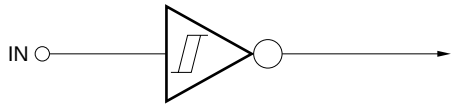
Pin	Alternate Function	I/O Circuit Type	I/O Buffer Power Supply	Recommended Connection Method
P121	SO4	10-G	V_{DD}	Input: Independently connect to V_{DD} or V_{SS} via a resistor Output: Leave open
P122	$\overline{SCK4}$	10-H		
P123	CLO	5		
P124	TI6/TO6	5-K		
P125	TI7/TO7			
P126	TI10/TO10			
P127	TI11/TO11			
P130 to P133	INTCP80 to INTCP83	5-K	V_{DD}	
P134	TI8/INTTI8			
P135	TCLR8/INTTCLR8			
P136, P137	TO80, TO81	5		
P140 to P143	INTCP90 to INTCP93	5-K	V_{DD}	
P144	TI9/INTTI9			
P145	RTPTRG1			
P146, P147	–	5		
P150 to P157	RTP10 to RTP17	5	V_{DD}	
P160 to P163	PWM0 to PWM3	5	V_{DD}	
P164	CSYNCIN	5-K		
P165	VSOUT	5		
P166	HSOUT0			
P167	HSOUT1			
P170 to P177	KR0 to KR7	5-K	V_{DD}	
P180 to P187	–	5	V_{DD}	
P190 to P197	–	5	V_{DD}	
CLKOUT	–	4	BV_{DD}	Leave open
$\overline{WAIT}$	–	1	BV_{DD}	Connect to V_{DD} via a resistor
$\overline{RESET}$	–	2	V_{DD}	–
X1	–	–	V_{DD}	–
X2	–	–	V_{DD}	Leave open
XT1	–	–	V_{DD}	Connect to V_{SS}
XT2	–	–	V_{DD}	Leave open
AV_{REF}	–	–	–	Connect to AV_{SS}
V_{PP}	–	–	–	Connect to V_{SS}
V_{DD}	–	–	–	–
V_{SS}	–	–	–	–
AV_{DD}	–	–	–	Connect to V_{DD}
AV_{SS}	–	–	–	Connect to V_{SS}
BV_{DD}	–	–	–	Connect to V_{DD}
BV_{SS}	–	–	–	Connect to V_{SS}

Figure 1-1. Pin Input/Output Circuits (1/2)

Type 1

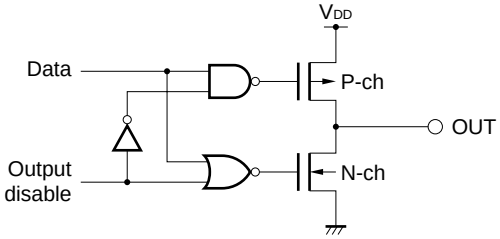


Type 2



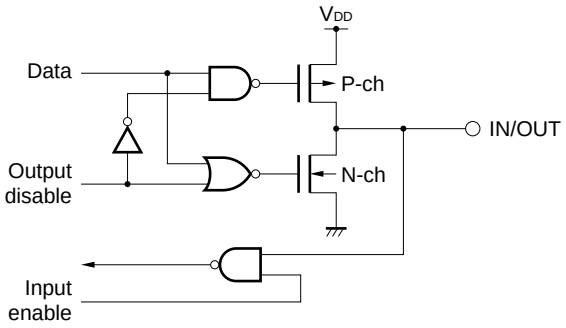
Schmitt-triggered input with hysteresis characteristics

Type 4

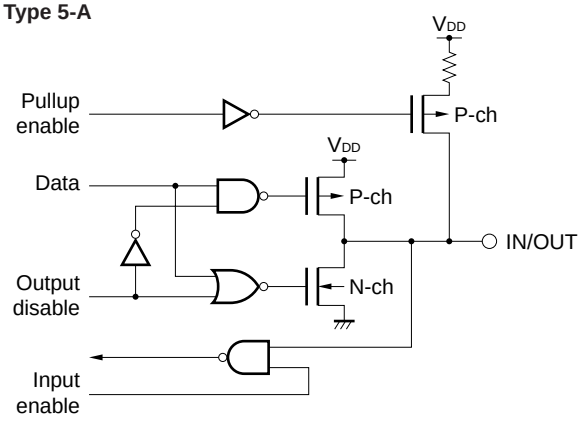


Push-pull output that can be set for high impedance output (both P-ch and N-ch are off)

Type 5



Type 5-A



Type 5-K

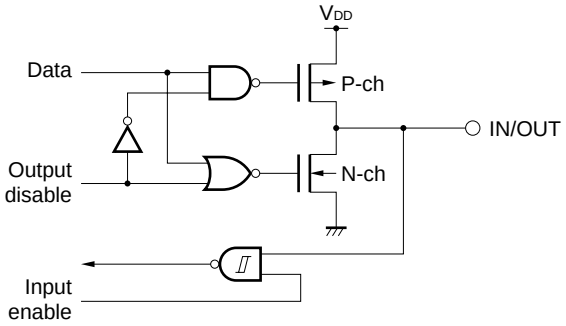
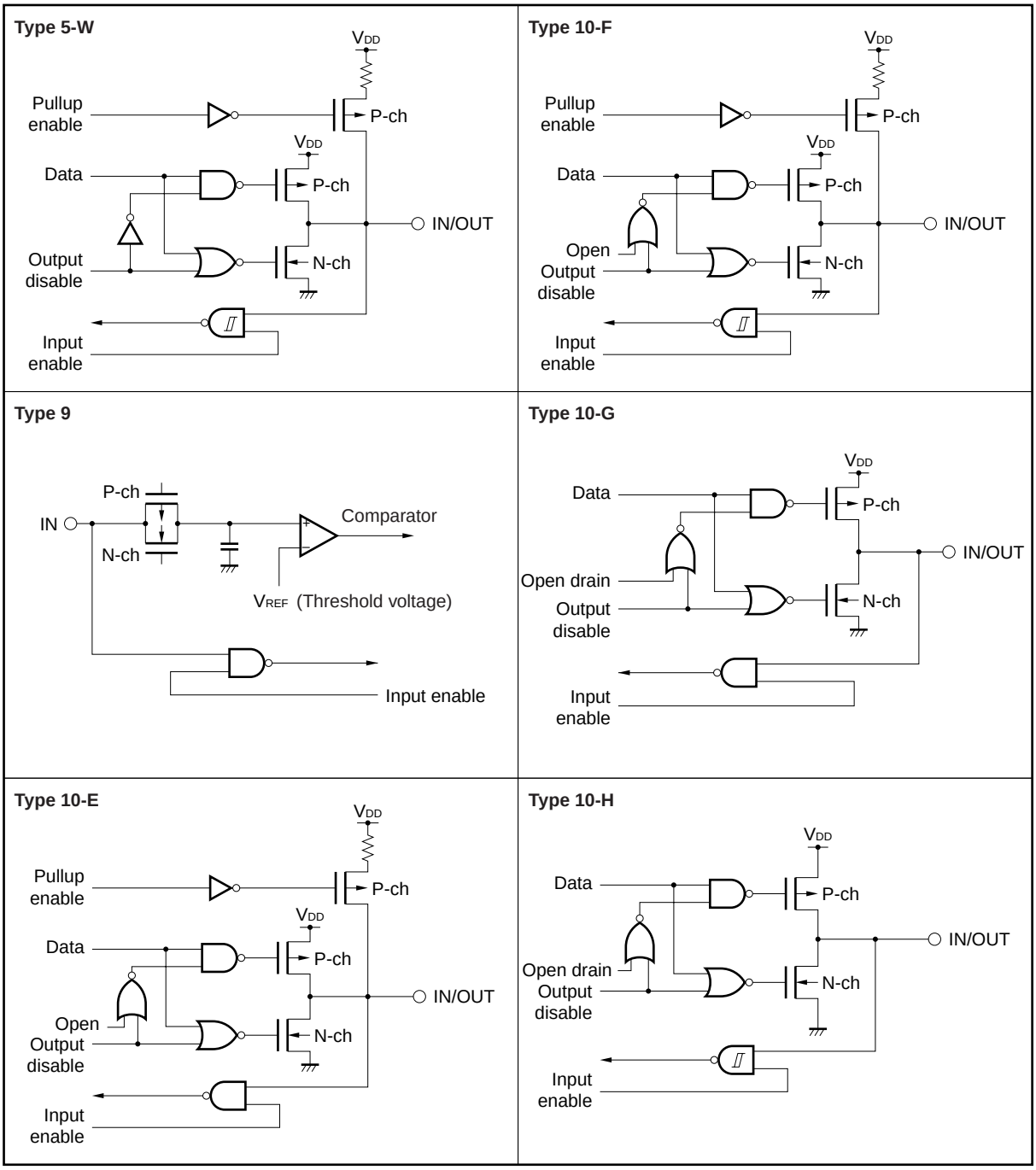


Figure 1-1. Pin Input/Output Circuits (2/2)



2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.5 to +4.6	V
	AV_{DD}		–0.5 to +4.6	V
	BV_{DD}		–0.5 to +4.6	V
	AV_{SS}		–0.5 to +0.5	V
	BV_{SS}		–0.5 to +0.5	V
Input voltage	V_{I1}	**Note 1** (V_{DD})	–0.5 to V_{DD} + 0.5[Note 4]	V
	V_{I2}	**Note 2** (BV_{DD})	–0.5 to BV_{DD} + 0.5[Note 4]	V
	V_{I3}	V_{PP}	–0.5 to +8.5	V
Clock input voltage	V_K	X1, XT1, V_{DD} = 2.7 to 3.6 V	–0.5 to V_{DD} + 1.0[Note 4]	V
Analog input voltage	V_{IAN}	**Note 3** (AV_{DD})	–0.5 to AV_{DD} + 0.5[Note 4]	V
Analog reference input voltage	AV_{REF}	AV_{REF} pin	–0.5 to AV_{DD} + 0.5[Note 4]	V
Output current, low	I_{OL}	Per pin	4.0	mA
		Total for P00 to P07 and P150 to P157	25	mA
		Total for P100 to P107 and P160 to P167	25	mA
		Total for P170 to P177 and P190 to P197	25	mA
		Total for P124 to P127 and P180 to P187	25	mA
		Total for P30 to P37 and P120 to P123	25	mA
		Total for P12 to P15, P20 to 27, and P110 to P113	25	mA
		Total for P50 to P57, P60 to P65, and CLKOUT	25	mA
		Total for P40 to P47 and P90 to P96	25	mA
		Total for P130 to P137 and P140 to P147	25	mA
Output current, high	I_{OH}	Per pin	–4.0	mA
		Total for P00 to P07 and P150 to P157	–25	mA
		Total for P100 to P107 and P160 to P167	–25	mA
		Total for P170 to P177 and P190 to P197	–25	mA
		Total for P124 to P127 and P180 to P187	–25	mA
		Total for P30 to P37 and P120 to P123	–25	mA
		Total for P12 to P15, P20 to 27, and P110 to P113	–25	mA
		Total for P50 to P57, P60 to P65, and CLKOUT	–25	mA
		Total for P40 to P47 and P90 to P96	–25	mA
		Total for P130 to P137 and P140 to P147	–25	mA
Output voltage	V_{O1}	**Note 1** (V_{DD})	–0.5 to V_{DD} + 0.5[Note 4]	V
	V_{O2}	**Note 2** (BV_{DD})	–0.5 to BV_{DD} + 0.5[Note 4]	V
Operating ambient temperature	T_A	Normal operation mode	–40 to +85	°C
		Flash programming mode	+10 to +40	°C
Storage temperature	T_{stg}		–40 to +125	°C

Notes 1. Ports 0, 1, 2, 3, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, $\overline{\text{RESET}}$ (including alternate-function pins)

2. Ports 4, 5, 6, 9, $\overline{\text{WAIT}}$ (including alternate-function pins)

3. Ports 7, 8 (including alternate-function pins)

4. Be sure not to exceed each absolute maximum rating (MAX.).

Cautions 1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND. However, direct connections among open-drain and open-connector pins are possible, as are direct connections to external circuits that have timing designed to prevent output contention with pins that become high-impedance.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz Unmeasured pins returned to 0 V			15	pF
I/O capacitance	C_{IO}				15	pF
Output capacitance	C_O				15	pF

Operating Conditions

(1) CPU Operation Frequency

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU operation frequency	f_{CPU}	When main system clock is operating	0.5		16	MHz
		When subsystem clock is operating		32.768		kHz

(2) Supply Voltage

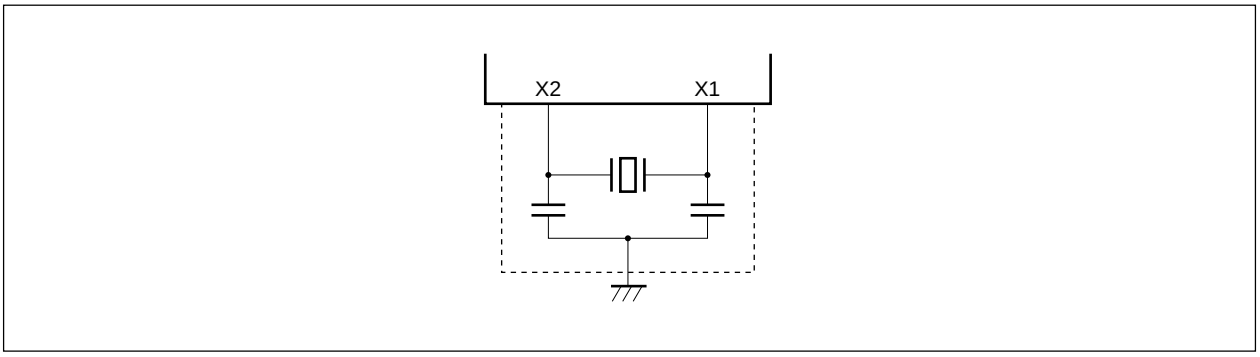
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		2.7		3.6	V
	AV_{DD}		2.7		3.6	V
	BV_{DD}		2.7		3.6	V

(3) Operating Frequency for Each Supply Voltage

Internal Operating Clock Frequency	Supply Voltage (V_{DD} = AV_{DD} = BV_{DD})
4 MHz ≤ f_{XX} ≤ 16 MHz	2.7 to 3.6 V
f_{XT} = 32.768 kHz	2.7 to 3.6 V

Recommended Oscillator

(1) Main System Clock Oscillator (T_A = –40 to +85°C)



Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	f_{XX}		4		16	MHz
Oscillation stabilization time		After reset release		$2^{19}/f_{XX}$		s
		After STOP mode release		**Note**		s

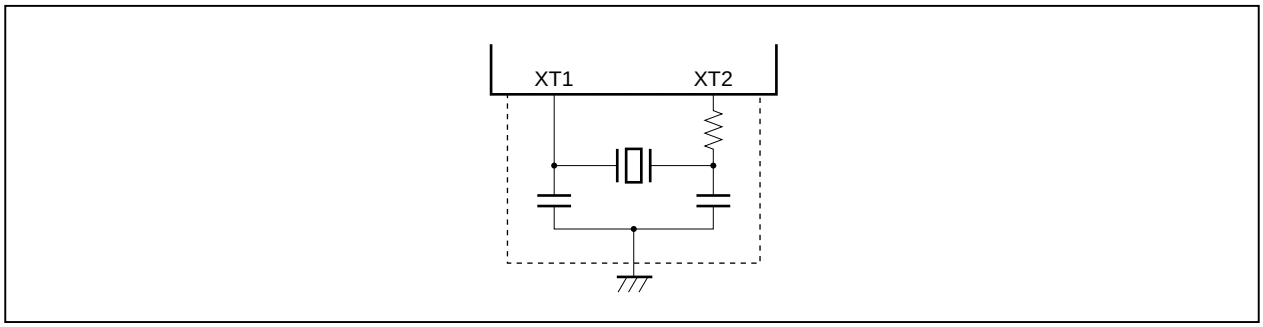
Note Values vary depending on the settings of the oscillation stabilization selection register (OSTS).

Remarks 1. Place the oscillator as close as possible to X1 and X2.

2. Do not wire other signal lines within the broken lines.

3. For resonator selection and oscillation constants, customers are advised to either evaluate the oscillation themselves, or apply to the resonator manufacturer for evaluation.

(2) Subsystem Clock Oscillator (T_A = –40 to +85°C)



Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	f_{XT}		32	32.768	35	kHz
Oscillation stabilization time				10		s

Remarks 1. Place the oscillator as close as possible to XT1 and XT2.

2. Do not wire other signal lines within the broken lines.

3. For resonator selection and oscillation constants, customers are advised to either evaluate the oscillation themselves, or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = AV_{SS} = BV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	Pins in **Note 1**, $\overline{WAIT}$		0.7BV_{DD}		BV_{DD}	V
	V_{IH2}	Pins in **Note 2**		0.7V_{DD}		V_{DD}	V
	V_{IH3}	Pins in **Note 3**, $\overline{RESET}$		0.75V_{DD}		V_{DD}	V
	V_{IH4}	Pins in **Note 4**		0.7AV_{DD}		AV_{DD}	V
	V_{IH5}	X1, XT1, XT2		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	Pins in **Note 1**, $\overline{WAIT}$		BV_{SS} – 0.5		0.3BV_{DD}	V
	V_{IL2}	Pins in **Note 2**		V_{SS} – 0.5		0.3V_{DD}	V
	V_{IL3}	Pins in **Note 3**, $\overline{RESET}$		V_{SS} – 0.5		0.3V_{DD}	V
	V_{IL4}	Pins in **Note 4**		AV_{SS} – 0.5		0.3AV_{DD}	V
	V_{IL5}	X1, XT1, XT2		V_{SS}		0.2V_{DD}	V
Output voltage, high	V_{OH1}	**Note 1**, CLKOUT	I_{OH} = –3 mA	0.8BV_{DD}			V
	V_{OH2}	**Notes 2, 3**	I_{OH} = –1 mA	0.8V_{DD}			V
Output voltage, low	V_{OL1}	**Note 1**, CLKOUT				0.4	V
	V_{OL2}	**Notes 2, 3** (excluding P10, 12, 20, 22)				0.4	V
	V_{OL3}	P10, 12, 20, 22				0.4	V
Input leakage current, high	I_{LIH1}	V_I = V_{DD} = AV_{DD} = BV_{DD}	Other than X1, XT1, XT2			5	μA
	I_{LIH2}		X1, XT1, XT2			20	μA
Input leakage current, low	I_{LIL1}	V_I = 0 V	Other than X1, XT1, XT2			–5	μA
	I_{LIL2}		X1, XT1, XT2			–20	μA
Output leakage current, high	I_{LOH}	V_O = V_{DD} = AV_{DD} = BV_{DD}				5	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–5	μA
Supply current	I_{DD1}	Normal operation (f_{XX} = 16 MHz)			45	65	mA
	I_{DD2}	HALT mode (f_{XX} = 16 MHz)			20	35	mA
	I_{DD3}	IDLE mode (f_{XX} = 16 MHz)			6	14	mA
	I_{DD4}	STOP mode (subsystem clock operation: f_{XT} = 32.768 kHz, watch timer operation			13	115	μA
		STOP mode (subsystem clock stopped)			1	100	μA
Pull-up resistor	R_L			10	30	100	kΩ

Notes 1. Ports 4, 5, 6, 9 (including alternate-function pins)

2. P11, P14, P21, P24, P34, P35, P100 to P107, P110 to P113, P121, P123, P136, P137, P146, P147, P150 to P157, P160 to P163, P165 to P167, P180 to P187, P190 to P197 (including alternate-function pins)

3. P00 to P07, P10, P12, P13, P15, P20, P22, P23, P25 to P27, P30 to P33, P36, P37, P120, P122, P124 to P127, P130 to P135, P140 to P145, P164, P170 to P177 (including alternate-function pins)

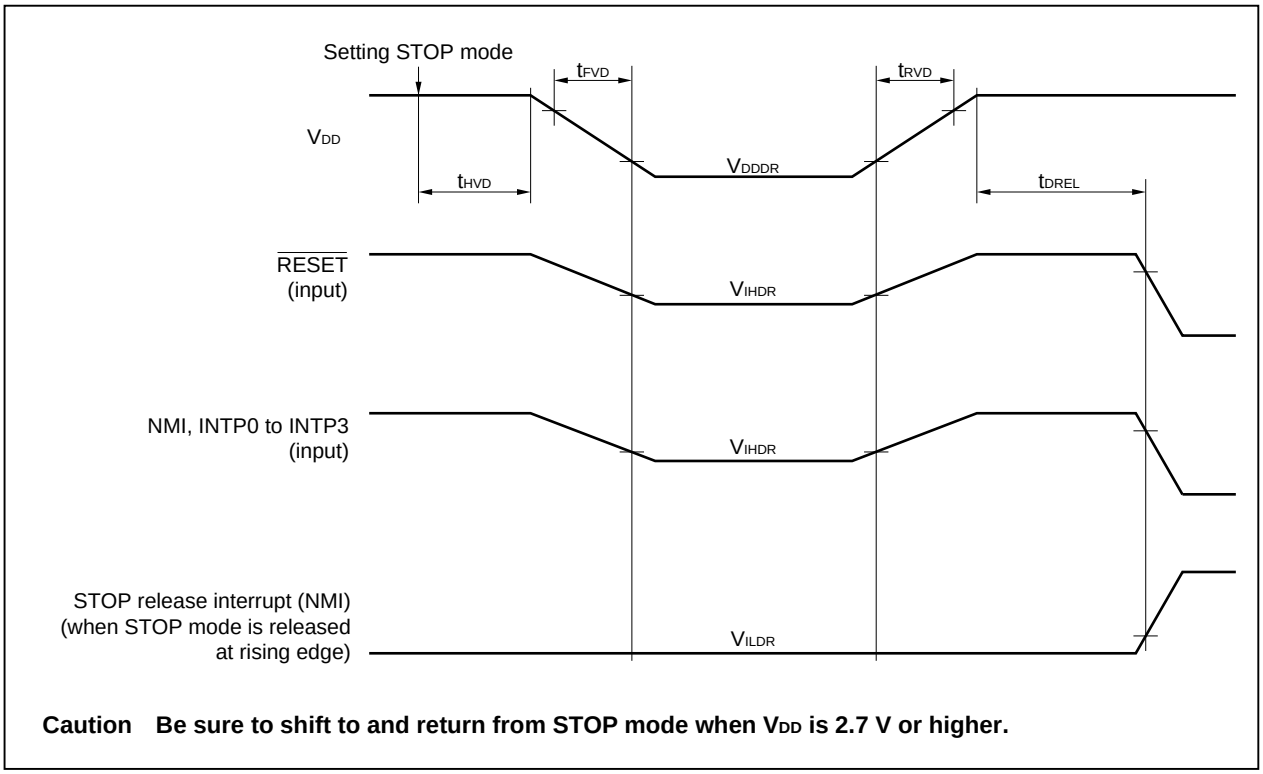
4. Ports 7, 8 (including alternate-function pins)

Caution The TYP. value of V_{DD} is 3.3 V. The current that is consumed at output buffers is not included.

Data Retention Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = AV_{SS} = BV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode	1.8		3.6	V
Data retention current	I_{DDDR}	V_{DDDR} [V]		1	100	μA
Supply voltage rise time	t_{RVD}		200			μs
Supply voltage fall time	t_{FVD}		200			μs
Supply voltage hold time (from STOP mode setting)	t_{HVD}		0			ms
STOP release signal input time	t_{DREL}		0			ms
Data retention high-level input voltage	V_{IHDR}	All input ports	V_{IHn}		V_{DDDR}	V
Data retention low-level input voltage	V_{ILDR}	All input ports	0		V_{ILn}	V

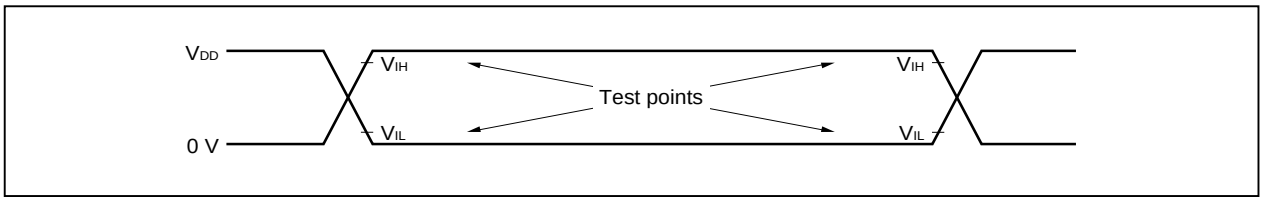
Remark n = 1 to 5



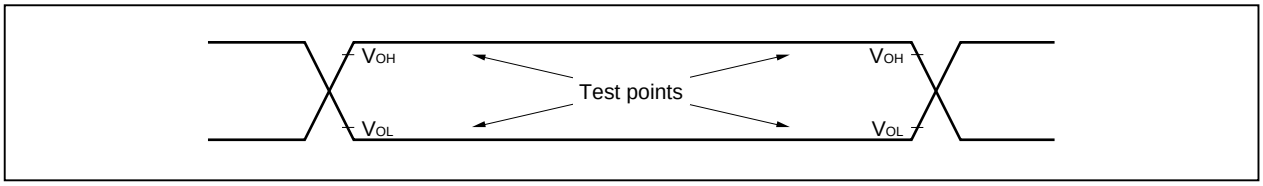
Caution Be sure to shift to and return from STOP mode when V_{DD} is 2.7 V or higher.

AC Characteristics

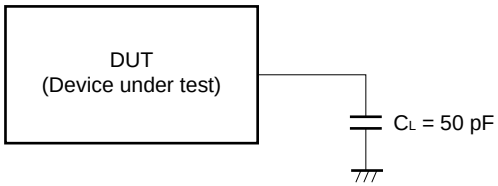
AC Test Input Waveforms (V_{DD}, BV_{DD}, AV_{DD})



AC Test Output Test Point (BV_{DD})



Load Conditions



Caution If the load capacitance exceeds 50 pF due to the circuit configuration, bring the load capacitance of the device to 50 pF or less by inserting a buffer or by some other means.

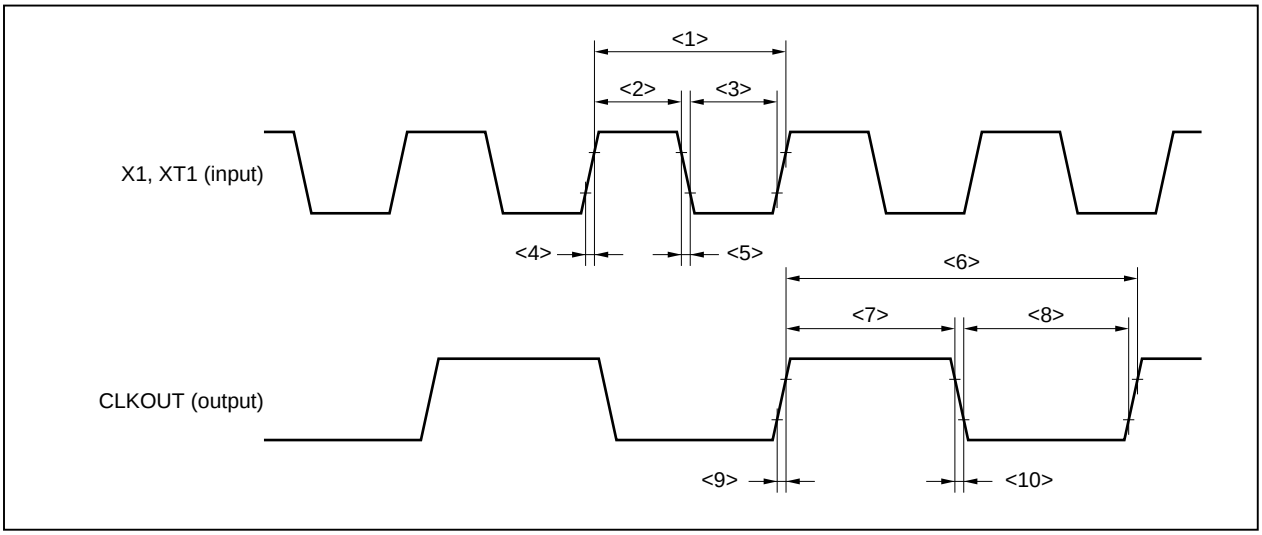
Clock Timing

Operating Condition (T_A = –40 to +85°C, V_{DD} = AV_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = AV_{SS} = BV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
X1 input cycle	t_{CYX}	<1>		62.5	250	ns
XT1 input cycle				28.6	31.2	μs
X1 input high-level width	t_{WXH}	<2>		31.2	125	ns
XT1 input high-level width				14.3	15.6	μs
X1 input low-level width	t_{WXL}	<3>		31.2	125	ns
XT1 input low-level width				14.3	15.6	μs
X1 input rise time	t_{XR}	<4>			(<1>–<2>–<3>)/2	ns
X1 input fall time	t_{XF}	<5>			(<1>–<2>–<3>)/2	ns
CLKOUT output cycle	t_{CYK}	<6>		62.5 ns	31.2 μs	
CLKOUT high-level width	t_{WKH}	<7>		0.4 (T–20)		ns
CLKOUT low-level width	t_{WKL}	<8>		0.4 (T–20)		ns
CLKOUT rise time	t_{KR}	<9>			10	ns
CLKOUT fall time	t_{KF}	<10>			10	ns

Remark T = t_{CYK}

Clock Timing



Timing of Pins Other Than X1 and CLKOUT Pins

(T_A = –40 to +85°C, V_{DD} = AV_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = AV_{SS} = BV_{SS} = 0 V, Output Pin Load Capacitance: C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output rise time	t_{OR}			20	ns
Output fall time	t_{OF}			20	ns

Bus Timing (CLKOUT Asynchronous)

(T_A = –40 to +85°C, V_{DD} = AV_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = AV_{SS} = BV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to ASTB↓)	t_{SAST}	<11>		0.5T – 20		ns
Address hold time (from ASTB↓)	t_{HSTA}	<12>		0.5T – 15		ns
Address float from $\overline{DSTB}$↓	t_{FDA}	<13>			2	ns
Setup time from address to data input	t_{DAID}	<14>			(2 + n)T – 30	ns
Setup time from $\overline{DSTB}$↓ to data input	t_{DDID}	<15>			(1 + n)T – 30	ns
Delay time from ASTB↓ to $\overline{DSTB}$↓	t_{DSTD}	<16>		0.5T – 15		ns
Data input hold time (from $\overline{DSTB}$↑)	t_{HDID}	<17>		0		ns
Address output time from $\overline{DSTB}$↑	t_{DDA}	<18>		(1 + i)T – 15		ns
Delay time from $\overline{DSTB}$↑ to ASTB↑	t_{DDST1}	<19>		0.5T – 15		ns
Delay time from $\overline{DSTB}$↑ to ASTB↓	t_{DDST2}	<20>		(1.5 + i)T – 15		ns
$\overline{DSTB}$ low-level width	t_{WDL}	<21>		(1 + n)T – 15		ns
ASTB high-level width	t_{WSTH}	<22>		T – 15		ns
Data output time from $\overline{DSTB}$↓	t_{DDOD}	<23>			15	ns
Data output setup time (to $\overline{DSTB}$↑)	t_{SODD}	<24>		(1 + n)T – 20		ns
Data output hold time (from $\overline{DSTB}$↑)	t_{HDOD}	<25>		T – 15		ns
$\overline{WAIT}$ setup time (to address)	t_{SAWT1}	<26>	n ≥ 1		1.5T – 30	ns
	t_{SAWT2}	<27>			(1.5 + n)T – 30	ns
$\overline{WAIT}$ hold time (from address)	t_{HAWT1}	<28>	n ≥ 1	(0.5 + n)T		ns
	t_{HAWT2}	<29>		(1.5 + n)T		ns
$\overline{WAIT}$ setup time (to ASTB↓)	t_{SSTWT1}	<30>	n ≥ 1		1.5T – 25	ns
	t_{SSTWT2}	<31>			(1 + n)T – 5	ns
$\overline{WAIT}$ hold time (from ASTB↓)	t_{HSTWT1}	<32>	n ≥ 1	nT + 5		ns
	t_{HSTWT2}	<33>		(1 + n)T + 5		ns
$\overline{HLDRQ}$ high-level width	t_{WHQH}	<34>		T + 10		ns
$\overline{HLDAK}$ low-level width	t_{WHAL}	<35>		T – 15		ns
Delay time from $\overline{HLDAK}$↑ to bus output	t_{DHAC}	<36>		0		ns
Delay time from $\overline{HLDRQ}$↓ to $\overline{HLDAK}$↓	t_{DHQHA1}	<37>		1.5T	(2n + 7.5)T + 25	ns
Delay time from $\overline{HLDRQ}$↑ to $\overline{HLDAK}$↑	t_{DHQHA2}	<38>		0.5T	1.5T + 25	ns

Remarks 1. T = 1/f_{CPU} (f_{CPU}: CPU operation clock frequency)

2. n: Number of wait clocks inserted in the bus cycle.
Sampling timing changes when a programmable wait is inserted.

3. i: Number of idle states inserted after the read cycle (0 or 1).

4. The specifications described above are the values of when a clock with a duty ratio of 1:1 is input from X1.

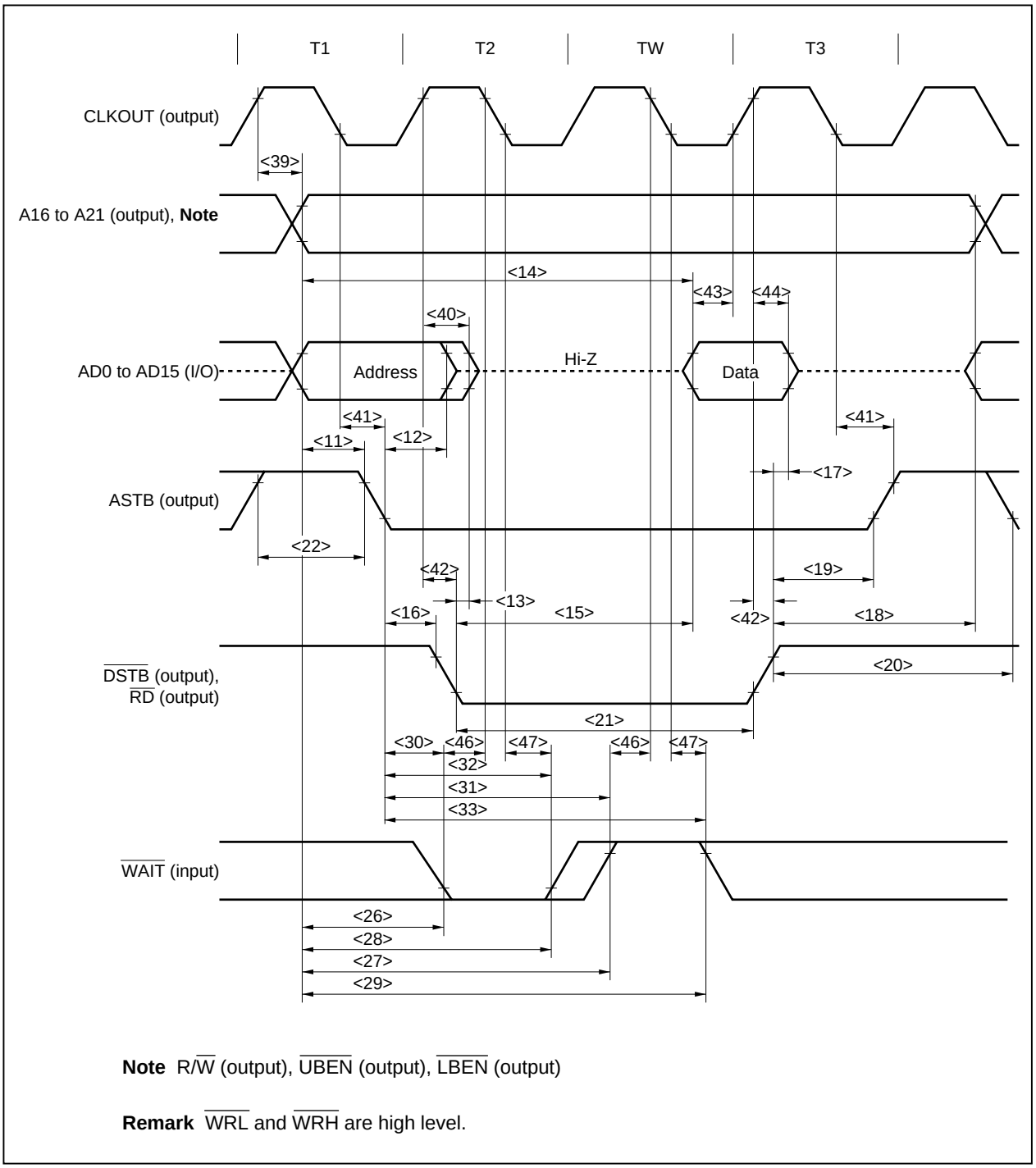
Bus Timing (CLKOUT Synchronous)

(T_A = –40 to +85°C, V_{DD} = AV_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = AV_{SS} = BV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	t_{DKA}	<39>		0	19	ns
Delay time from CLKOUT↑ to address float	t_{FKA}	<40>		–12	7	ns
Delay time from CLKOUT↓ to ASTB	t_{DKST}	<41>		–12	7	ns
Delay time from CLKOUT↑ to $\overline{DSTB}$	t_{DKD}	<42>		–5	14	ns
Data input setup time (to CLKOUT↑)	t_{SIDK}	<43>		15		ns
Data input hold time (from CLKOUT↑)	t_{HKID}	<44>		5		ns
Delay time from CLKOUT↑ to data output	t_{DKOD}	<45>			19	ns
$\overline{WAIT}$ setup time (to CLKOUT↓)	t_{SWTK}	<46>		15		ns
$\overline{WAIT}$ hold time (from CLKOUT↓)	t_{HKWT}	<47>		5		ns
$\overline{HLDRQ}$ setup time (to CLKOUT↓)	t_{SHQK}	<48>		15		ns
$\overline{HLDRQ}$ hold time (from CLKOUT↓)	t_{HKHQ}	<49>		5		ns
Delay time from CLKOUT↑ to address float	t_{DKF}	<50>			19	ns
Delay time from CLKOUT↑ to $\overline{HLDAK}$	t_{DKHA}	<51>			19	ns

Remark The specifications described above are the values of when a clock with a duty ratio of 1:1 is input from X1.

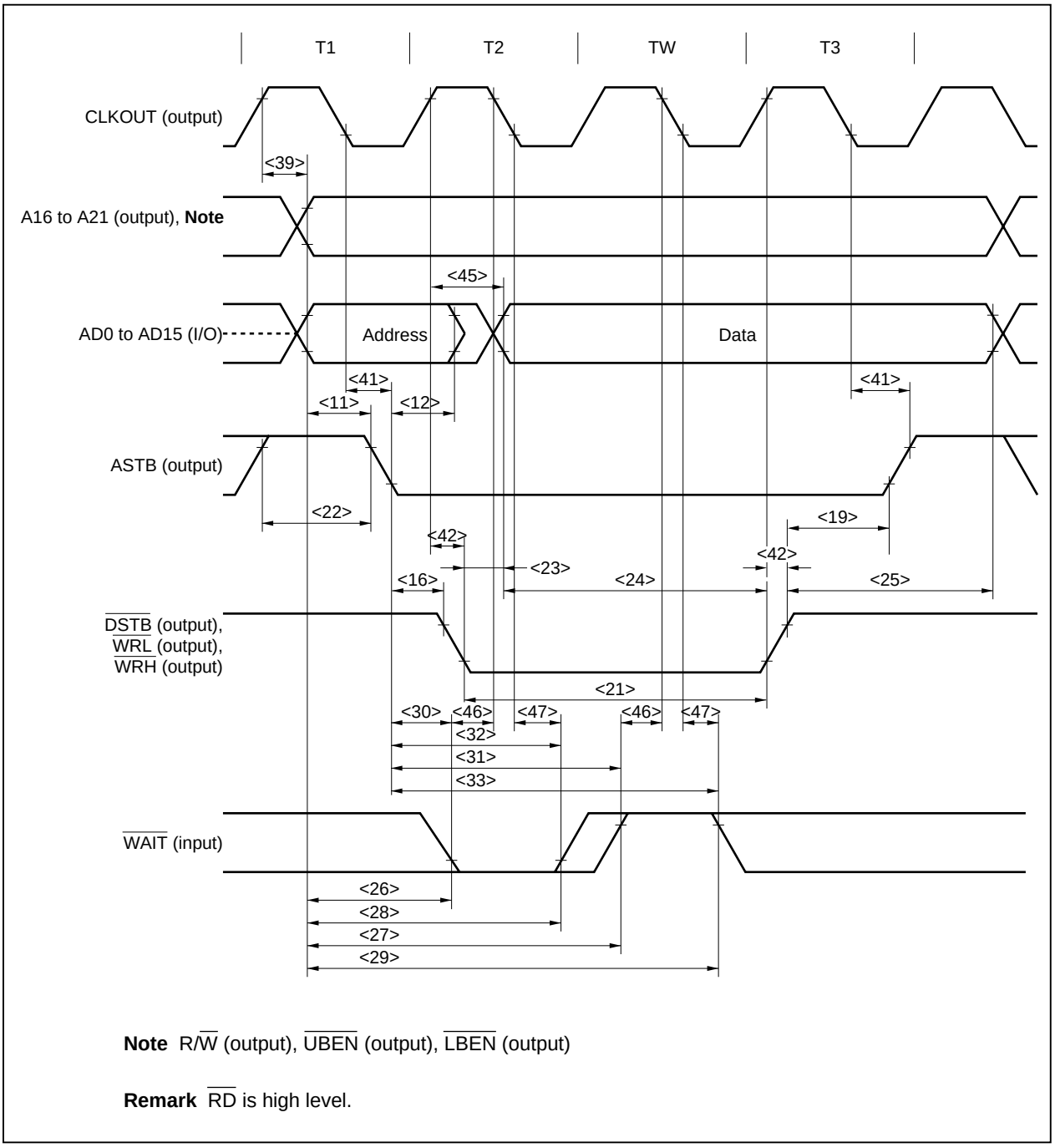
Read Cycle (CLKOUT Synchronous/Asynchronous, 1 Wait)



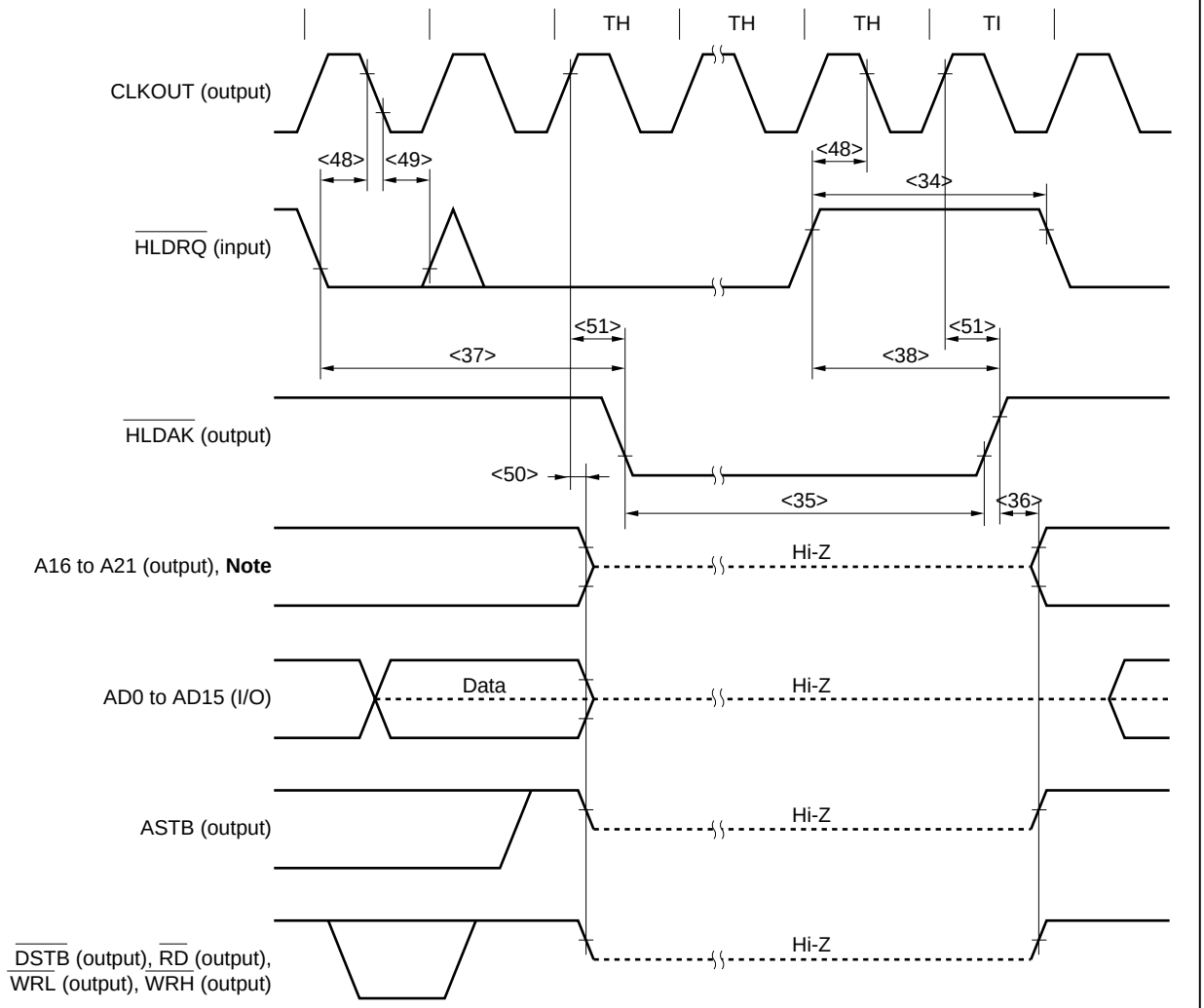
Note R/$\overline{W}$ (output), $\overline{UBEN}$ (output), $\overline{LBEN}$ (output)

Remark $\overline{WRL}$ and $\overline{WRH}$ are high level.

Write Cycle (CLKOUT Synchronous/Asynchronous, 1 Wait)



Bus Hold



Note R/W (output), UBEN (output), LBEN (output)

Reset/Interrupt Timing

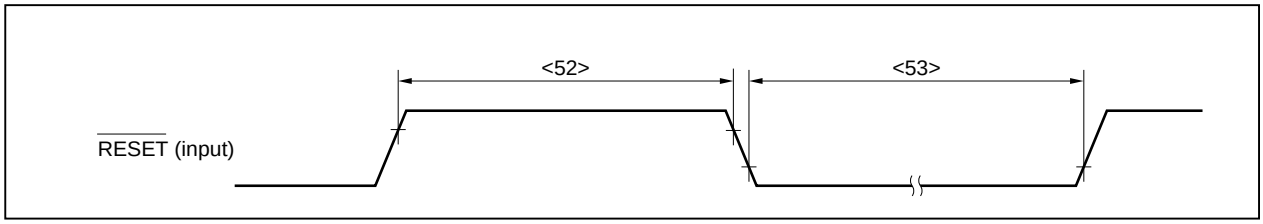
(T_A = –40 to +85°C, V_{DD} = AV_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = AV_{SS} = BV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ high-level width	t_{WRSH}	<52>		500		ns
$\overline{\text{RESET}}$ low-level width	t_{WRSL}	<53>		500		ns
NMI high-level width	t_{WNIH}	<54>		500		ns
NMI low-level width	t_{WNIL}	<55>		500		ns
INTPn high-level width	t_{WITH}	<56>	n = 0 to 3, analog noise elimination	500		ns
			n = 4, 5, digital noise elimination	3T + 20		ns
			n = 6, digital noise elimination	3Tsmp + 20		ns
INTPn low-level width	t_{WITL}	<57>	n = 0 to 3, analog noise elimination	500		ns
			n = 4, 5, digital noise elimination	3T + 20		ns
			n = 6, digital noise elimination	3Tsmp + 20		ns

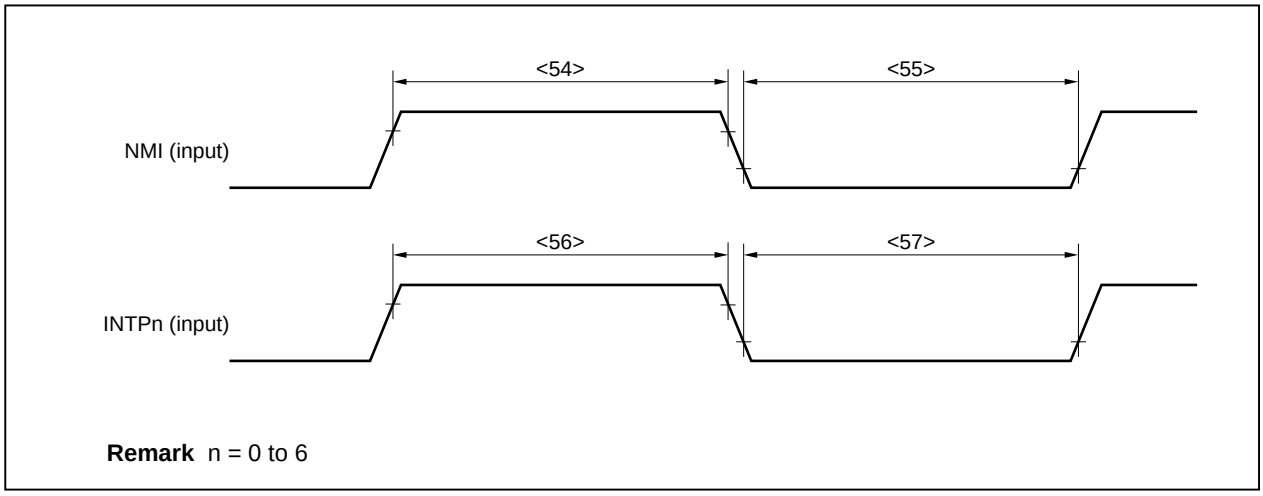
Remarks 1. T = 1/f_{XX}

2. Tsmp = Noise elimination sampling clock frequency

Reset



Interrupt



Remark n = 0 to 6

TIn Input Timing

(T_A = –40 to +85°C, V_{DD} = AV_{DD} =BV_{DD} = 2.7 to 3.6 V, V_{SS} = AV_{SS} = BV_{SS} = 0 V)

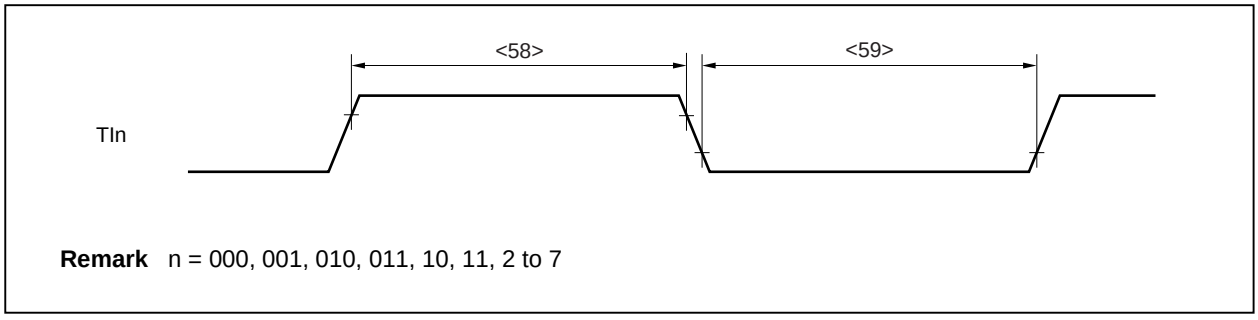
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
TIn0, TIn1 (n = 00, 01) High-level width	t_{TIIH}	<58>		$2T_{sam}$ + 20[Note]		ns
TIn (n = 2 to 7, 10, 11) High-level width				$3/f_{XX}$ + 20		ns
TIn0, TIn1 (n = 00, 01) Low-level width	t_{TIIL}	<59>		$2T_{sam}$ + 20[Note]		ns
TIn (n = 2 to 7, 10, 11) Low-level width				$3/f_{XX}$ + 20		ns

Note T_{sam} can be selected by setting the PRMn1 and PRMn0 bits of prescaler mode registers n0, n1 (PRMn0, PRMn1) (n = 0, 1).

TM0 (PRM00, PRM01 registers): T_{sam} = $2/f_{XX}$, $4/f_{XX}$, $16/f_{XX}$, $64/f_{XX}$, $256/f_{XX}$, 1/INTWTI period

TM1 (PRM10, PRM11 registers): T_{sam} = $2/f_{XX}$, $4/f_{XX}$, $16/f_{XX}$, $32/f_{XX}$, $128/f_{XX}$, $256/f_{XX}$

However, when the TIn0 valid edge is selected as the count clock, T_{sam} = $4/f_{XX}$ (n = 0, 1).



Remark n = 000, 001, 010, 011, 10, 11, 2 to 7

3-Wire SIO Timing

(1) Master Mode (T_A = –40 to +85°C, V_{DD} = AV_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = AV_{SS} = BV_{SS} = 0 V)

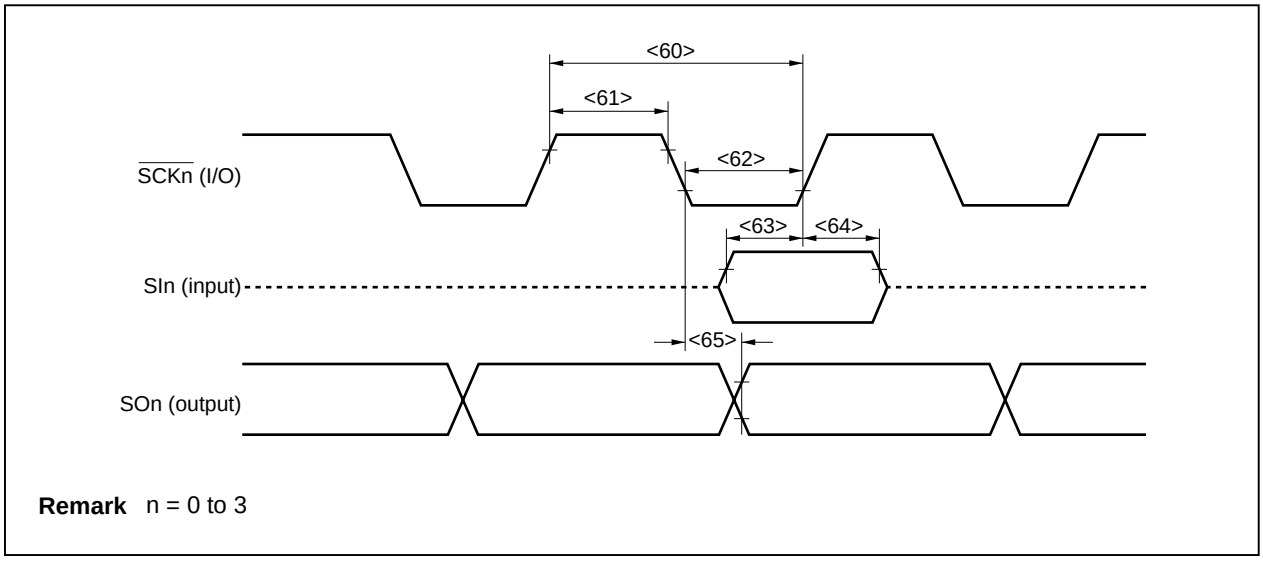
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle time	t_{KCY1}	<60>		400		ns
$\overline{SCKn}$ high-level width	t_{KH1}	<61>		140		ns
$\overline{SCKn}$ low-level width	t_{KL1}	<62>		140		ns
SIn setup time (to $\overline{SCKn}$↑)	t_{SIK1}	<63>		50		ns
SIn hold time (from $\overline{SCKn}$↓)	t_{KSI1}	<64>		50		ns
Delay time from $\overline{SCKn}$↓ to SOn output	t_{KSO1}	<65>			60	ns

Remark n = 0 to 3

(2) Slave Mode (T_A = –40 to +85°C, V_{DD} = AV_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = AV_{SS} = BV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle time	t_{KCY2}	<60>		400		ns
$\overline{SCKn}$ high-level width	t_{KH2}	<61>		140		ns
$\overline{SCKn}$ low-level width	t_{KL2}	<62>		140		ns
SIn setup time (to $\overline{SCKn}$↑)	t_{SIK2}	<63>		50		ns
SIn hold time (from $\overline{SCKn}$↓)	t_{KSI2}	<64>		50		ns
Delay time from $\overline{SCKn}$↓ to SOn output	t_{KSO2}	<65>			60	ns

Remark n = 0 to 3



Remark n = 0 to 3

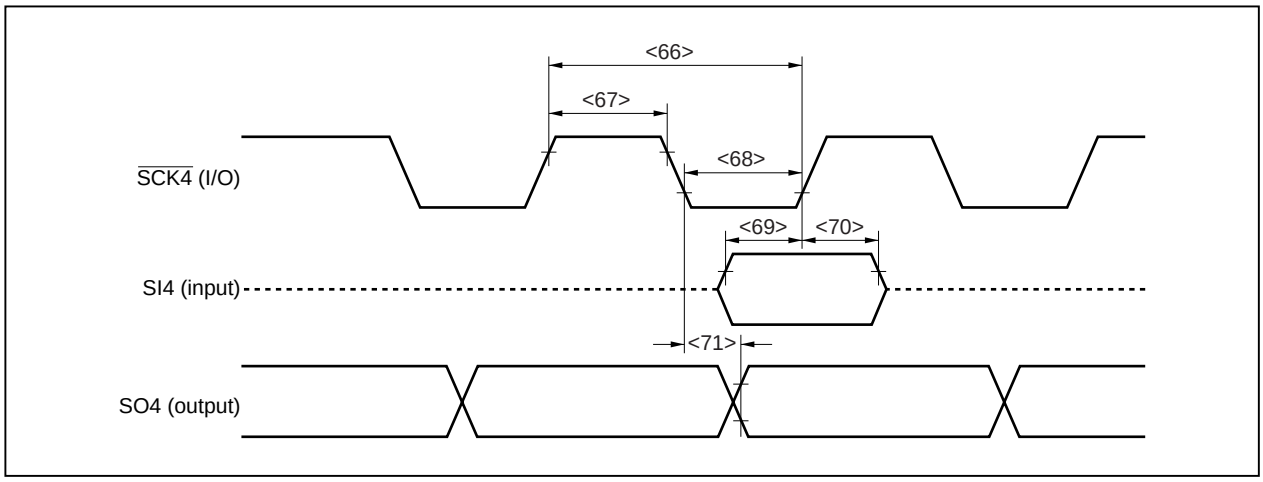
3-Wire Variable-Length CSI Timing

(1) Master Mode (T_A = –40 to +85°C, V_{DD} = AV_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = AV_{SS} = BV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCK4}$ cycle time	t_{KCY1}	<66>		400		ns
$\overline{SCK4}$ high-level width	t_{KH1}	<67>		140		ns
$\overline{SCK4}$ low-level width	t_{KL1}	<68>		140		ns
SI4 setup time (to $\overline{SCK4}$↑)	t_{SIK1}	<69>		50		ns
SI4 hold time (from $\overline{SCK4}$↑)	t_{KSI1}	<70>		50		ns
Delay time from $\overline{SCK4}$↓ to SO4 output	t_{KSO1}	<71>			60	ns

(2) Slave Mode (T_A = –40 to +85°C, V_{DD} = AV_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = AV_{SS} = BV_{SS} = 0 V)

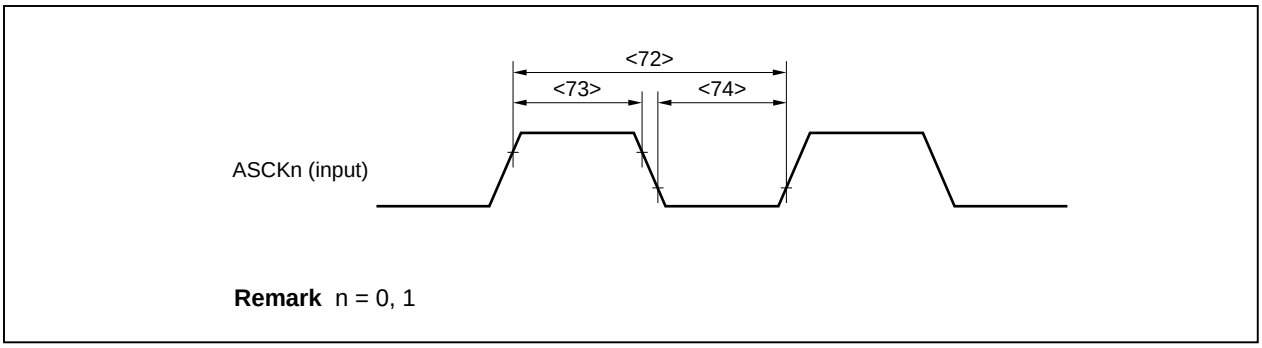
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCK4}$ cycle time	t_{KCY2}	<66>		400		ns
$\overline{SCK4}$ high-level width	t_{KH2}	<67>		140		ns
$\overline{SCK4}$ low-level width	t_{KL2}	<68>		140		ns
SI4 setup time (to $\overline{SCK4}$↑)	t_{SIK2}	<69>		50		ns
SI4 hold time (from $\overline{SCK4}$↑)	t_{KSI2}	<70>		50		ns
Delay time from $\overline{SCK4}$↓ to SO4 output	t_{KSO2}	<71>			60	ns



UART Timing (T_A = –40 to +85°C, V_{DD} = AV_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = AV_{SS} = BV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
ASCKn cycle time	t_{KCY13}	<72>		200		ns
ASCKn high-level width	t_{KH13}	<73>		80		ns
ASCKn low-level width	t_{KL13}	<74>		80		ns

Remark n = 0, 1



Remark n = 0, 1

I²C Bus Mode (Only for μPD70F3040Y)

(T_A = –40 to +85°C, V_{DD} = AV_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = AV_{SS} = BV_{SS} = 0 V)

Parameter		Symbol		Standard Mode		High-Speed Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLn clock frequency		f_{CLK}		0	100	0	400	kHz
Bus free time (between stop/start conditions)		t_{BUF}	<75>	4.7	–	1.3	–	μs
Hold time[Note 1]		$t_{HD:STA}$	<76>	4.0	–	0.6	–	μs
SCLn clock low-level width		t_{LOW}	<77>	4.7	–	1.3	–	μs
SCLn clock high-level width		t_{HIGH}	<78>	4.0	–	0.6	–	μs
Setup time of start/restart conditions		$t_{SU:STA}$	<79>	4.7	–	0.6	–	μs
Data hold time	CBUS-compatible master	$t_{HD:DAT}$	<80>	5.0	–	–	–	μs
	I²C mode			0[Note 2]	–	0[Note 2]	0.9[Note 3]	μs
Data setup time		$t_{SU:DAT}$	<81>	250	–	100[Note 4]	–	ns
Rising time of SDAn and SCLn signals		t_R	<82>	–	1000	20 + 0.1Cb[Note 5]	300	ns
Falling time of SDAn and SCLn signals		t_F	<83>	–	300	20 + 0.1Cb[Note 5]	300	ns
Setup time of stop condition		$t_{SU:STO}$	<84>	4.0	–	0.6	–	μs
Pulse width of spike suppressed by input filter		t_{SP}	<85>	–	–	0	50	ns
Load capacitance of bus line		Cb		–	400	–	400	pF

Notes 1. The first clock pulse in the start condition is generated after the hold time.

2. The system must internally provide at least 300-ns hold time for the SDAn signal (at $V_{IHmin.}$ of the SCLn signal) in order to fill the undefined period that appears at the SCLn falling edge.

3. If the system does not extend the low hold time (t_{LOW}), it is required to satisfy only the maximum data hold time ($t_{HD:DAT}$).

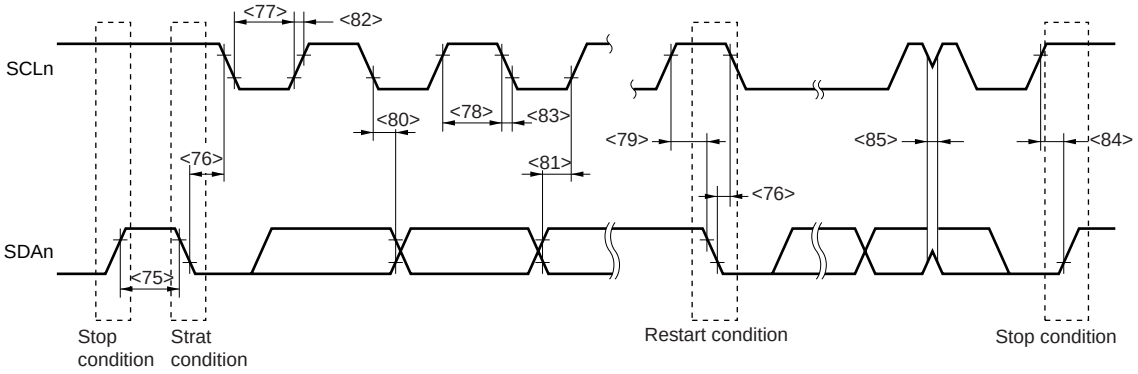
4. The high-speed I²C bus is available in the standard mode I²C bus system. In this case, following conditions should be satisfied.

- When the system does not extend the low-state hold time of the SCLn signal
  $t_{SU:DAT} \geq 250$ ns
- When the system extends the low-state hold time of the SCLn signal
  Before the SCLn line is released ($t_{Rmax.} + t_{SU:DAT}$ = 1000 + 250 = 1250 ns: Standard mode I²C bus specification), send the next data bit to the SDAn line.

5. Cb: Total capacitance of one bus line (Unit: pF)

Remark n = 0, 1

I²C Bus Mode (μPD70F3040Y only)



Remark n = 0, 1

A/D Converter (T_A = –40 to +85°C, V_{DD} = AV_{DD} = AV_{REF} = 2.7 to 3.6 V, AV_{SS} = V_{SS} = 0 V, Output Pin Load Capacitance: C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error Note 1					±0.8	%FSR
Conversion time	t_{CONV}		5		100	μs
Zero-scale error Note 1					±0.4	%FSR
Full-scale error Note 1					±0.4	%FSR
Integral linearity error Note 2					±4.0	LSB
Differential linearity error Note 2					±4.0	LSB
Analog reference voltage	AV_{REF}	AV_{REF} = AV_{DD}	2.7		3.6	V
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
AV_{REF} current	AI_{REF}			240	360	μA
Supply current	AI_{DD}			1	3	mA

Notes 1. Excluding quantization error (±0.05%FSR)

2. Excluding quantization error (±0.5LSB)

Remark LSB: Least Significant Bit
FSR: Full Scale Range

Flash Memory Programming Mode

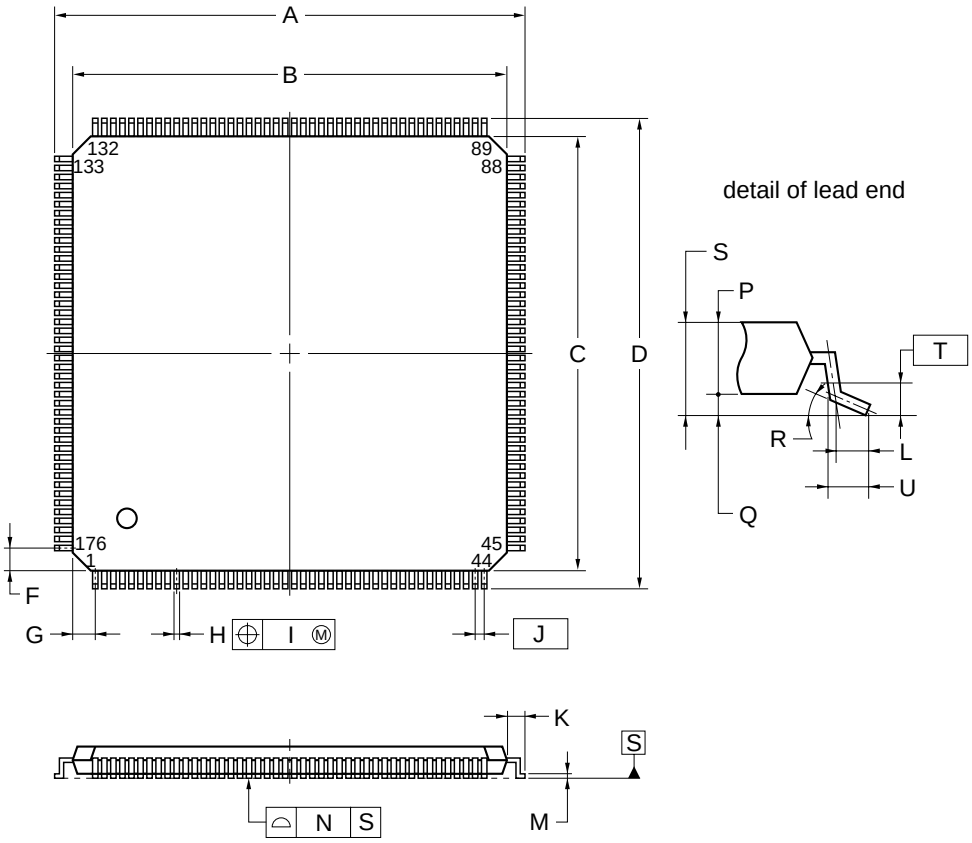
Write/Erase Characteristics (T_A = 10 to 40°C, V_{DD} = 3.0 to 3.6 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Write current	I_{DDW}	When $V_{PP} = V_{PP1}$	V_{DD} pin			67	mA
	I_{PPW}		V_{PP} pin			100	mA
Erase current	I_{DDE}	When $V_{PP} = V_{PP1}$	V_{DD} pin			67	mA
	I_{PPE}		V_{PP} pin			200	mA
Unit erase time	t_{ER}			0.2	0.2	0.2	s
Total erase time	t_{ERT}					20	s
Rewrite count[Note]				20	20	20	times
V_{PP} supply voltage	V_{PP0}	In normal operation mode		0		0.2V_{DD}	V
	V_{PP1}	In flash memory programming mode		7.5	7.8	8.1	V
Operation frequency				4		16	MHz

Note Write/erase is regarded as 1 cycle.

3. PACKAGE DRAWING

176-PIN PLASTIC LQFP (FINE PITCH) (24x24)



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	26.0±0.2
B	24.0±0.2
C	24.0±0.2
D	26.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.4
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.5±0.1

S176GM-50-UEU

4. RECOMMENDED SOLDERING CONDITIONS

T.B.D.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Related document μPD703039, 703039Y, 703040, 703040Y, 703041, 703041Y Data Sheet (U13953E)

Reference document Electrical Characteristics for Microcomputer (IEI-601) **Note**

Note This document number is that of the Japanese version.

The documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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